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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,686	07/07/2003	Jean-Pierre Schoellkopf	S1022.81020US00	7411

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/614,686	SCHOELLKOPF, JEAN-PIERRE	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *1-6 and 12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-11 and 13-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 7-11 and 13-17 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There is no support for a circuit comprising insulating portions covering the edges of the metal regions of determined pairs, wherein the edges of at least one pair of the metal regions not being covered by the insulating portions, as recite in claim 7, since the insulating portions covering all the edges of the metal regions of determined pairs, as depicted in figure 1D.

There is no adequate description in the disclosure for the claimed limitations of "at least one insulating portion covering the facing edges of at least one first pair of the pairs of metal regions so as to encode at least one first bit having a first polarity; and metal portions that cover the facing edges and connect at least one second pair of the pairs of metal regions so as to encode at least one second bit having a second polarity", as recited in claim 11.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 7-11 and 13-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claimed limitations of an integrated circuit comprising a stack of insulating layers, each layer being associated with a determined metallization level, metal areas of the last and uppermost metallization level forming electric contacts of the integrated circuit, comprising, as recited in claims 7 and 9, are unclear as to which element the second "comprising" term refers.

The claimed limitations of "the insulating portions associated with the determined pairs being interposed between the metal edges of the metal regions of the determined pairs and the associated covering metal portions of the last metallization layer;", as recited in claim 7, are unclear as to the exact location of the insulating portions associated with the determined pairs. It is further unclear as to which element is "the associated covering metal portions of the last metallization layer".

The claimed limitations of "metal portions of the uppermost metallization level which cover the facing edges of the metal regions of all pairs and which connect, for at least one pair of metal regions, the metal regions of the pairs other than the determined pairs", as recite in claim 9, are unclear as to how the phrase "for at least one pair of metal regions" modifies the structure of "metal portions of the uppermost metallization

level which cover the facing edges of the metal regions of all pairs and which connect the metal regions of the pairs other than the determined pairs".

The claimed limitations of "at least one insulating portion covering the facing edges of at least one first pair of the pairs of metal regions so as to encode at least one first bit having a first polarity; and metal portions that cover the facing edges and connect at least one second pair of the pairs of metal regions so as to encode at least one second bit having a second polarity", as recited in claim 11, are unclear as to what is meant by a first polarity and a second polarity, how an insulating portion encodes at least one first bit and how metal portions encode at least one second bit.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> **(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.**

Claims 7-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Ishimaru (6,656,826).

Ishimaru teaches in figure 1 and related text an integrated circuit adapted to specific needs, comprising a stack of insulating layers 3, 4, each layer being associated with a

determined metallization level 1, 2, metal areas of the last and uppermost metallization level forming electric contacts of the integrated circuit, comprising:

pairs of metal regions 2 of the penultimate metallization level having a facing edge and connected to components of the integrated circuit;

insulating portions 6 covering the edges of the metal regions of determined pairs according to the specific needs, the edges (located in the middle of metal region 2) of at least one pair of the metal regions not being covered by the insulating portions; and metal portions 8 of the last metallization level which cover the facing edges of the metal regions of all pairs and which connect the metal regions of the pairs other than the determined pairs, the insulating portions associated with the determined pairs being interposed between the metal edges of the metal regions of the determined pairs and the associated covering metal portions of the last metallization layer, and

a passivation layer 10, 11 covering the metal portions.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishimaru in view of Applicant Admitted Prior Art (AAPA).

Ishimaru teaches substantially the entire claimed structure, as recited in claims 7-8 above, except at least one insulating portion used to encode at least one first bit having a first polarity, and metal portions used to encode at least one second bit having a second polarity.

AAPA teaches in paragraphs [004] to [008] coding data in integrated circuits.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the at least one insulating portion to encode at least one first bit having a first polarity, and the metal portions to encode at least one second bit having a second polarity, in Ishimaru's device in order to use the device in an application which requires encoding data.

Regarding claims 16-17, the integrated circuit of prior art's device encodes a code having a plurality of bits, each bit being encoded by whether or not a pair of the metal regions is connected, wherein the integrated circuit hinders detection of the code by visual methods.

Response to Arguments

Applicant's arguments with respect to claims 7-11 and 13-17 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
3/16/07

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PRIMARY EXAMINER
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